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Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, May 2013
(2008 Scheme)
08.602 : VLSI DESIGN (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Explain the slicing and polishing of silicon wafers and the purpose of notch on the wafer.
2. Compare the properties of a n-type diffused layer and an epitaxial layer.
3. What is Electron beam lithography ?
4. Describe the techniques of isolation in IC fabrication.
5. Write down the secondary effects of MOSFET.
6. Implement the logic function F – [(A+B)C + DE] fusing static CMOS logic.
7. What is a transmission gate ? Draw XOR gate using T.G.
8. What are the design rules for layout ?
9. Explain carry look ahead adder.
10. With the help of a circuit diagram give proper explanation for the configuration of a 4×4 NOR – ROM array.

P.T.O.

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. Explain the process sequence of n-well CMOS inverter fabrication. Show the topview (mask) and cross section.

12. Explain the CZ and FZ process for crystal growth and compare them.

13. a) Explain an oxidation growth mechanism with a neat diagram.

    b) Explain the Deal Grove model of oxidation.

Module – II

14. a) What is scaling ? What are the different types of scaling ?

    b) Explain the different scaling effects in detail.

15. a) Explain the dynamic and static power dissipation in CMOS.

    b) Calculate the dynamic power dissipation in a chip operating with a V_{dd} of 5 V at 100 MHz with an internal switched capacitance of 300 pF.

16. Explain the CMOS inverter DC characteristics with the region of operation in detail.

Module – III

17. Explain square root carry select adder and derive the expression for time delay and compare its performance with other adders.

18. Draw the circuit diagram of a sense amplifier and give explanation on how the sensing of operation is carried out in SRAM cell.

19. a) What are the methods of design for testability ?

    b) Write short note on FPGAs.